Chair of Network Architectures and Services
Department of Computer Engineering
Technical University of Munich

Reproducible Research for Networked Systems

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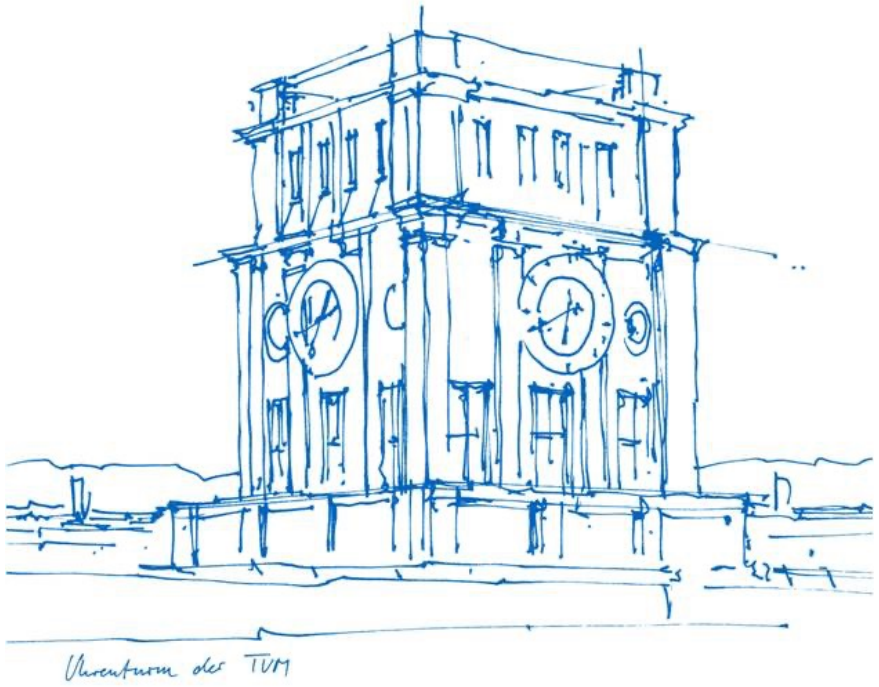
Acknowledgements:
All members of the Chair of
Network Architectures and Services



Outline

Needs

- Scalable, Resilient and Trustworthy Programmable Networked Systems with Predictable Performance
- Research Infrastructure for Reproducible Experiments

Challenges

Approach

- Framework, Methods and Tools for Reproducible Experiments

Conclusions

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Scalable, Resilient and Trustworthy Programmable Networked Systems

Need for Resilient Low-Latency Predictable Network Services

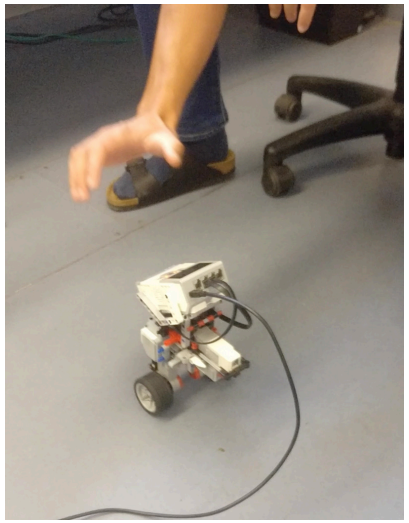
Challenges

- complex architectures
- performance, safety and security requirements

⇨ Need for

- Secure communication, trustworthy implementation
- Network stack + applications: *worst case performance guarantees*
- Scalability, flexibility, affordability, time-to-market

Low-Latency Systems:



Network-Controlled Robot

Power Grid Control

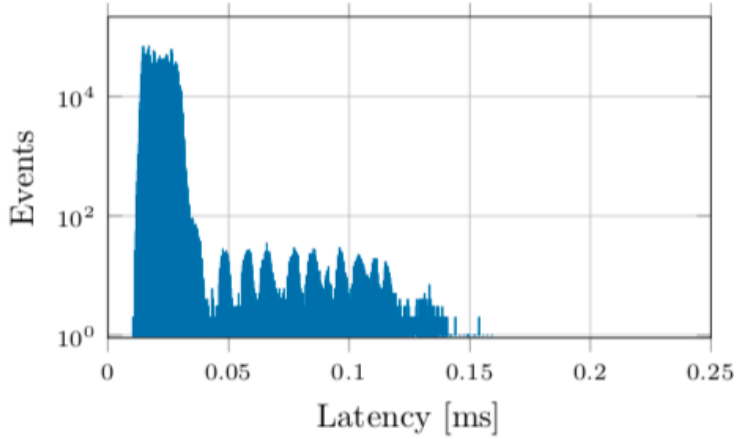
Need: End-to-End Worst-Case Latency Guarantees

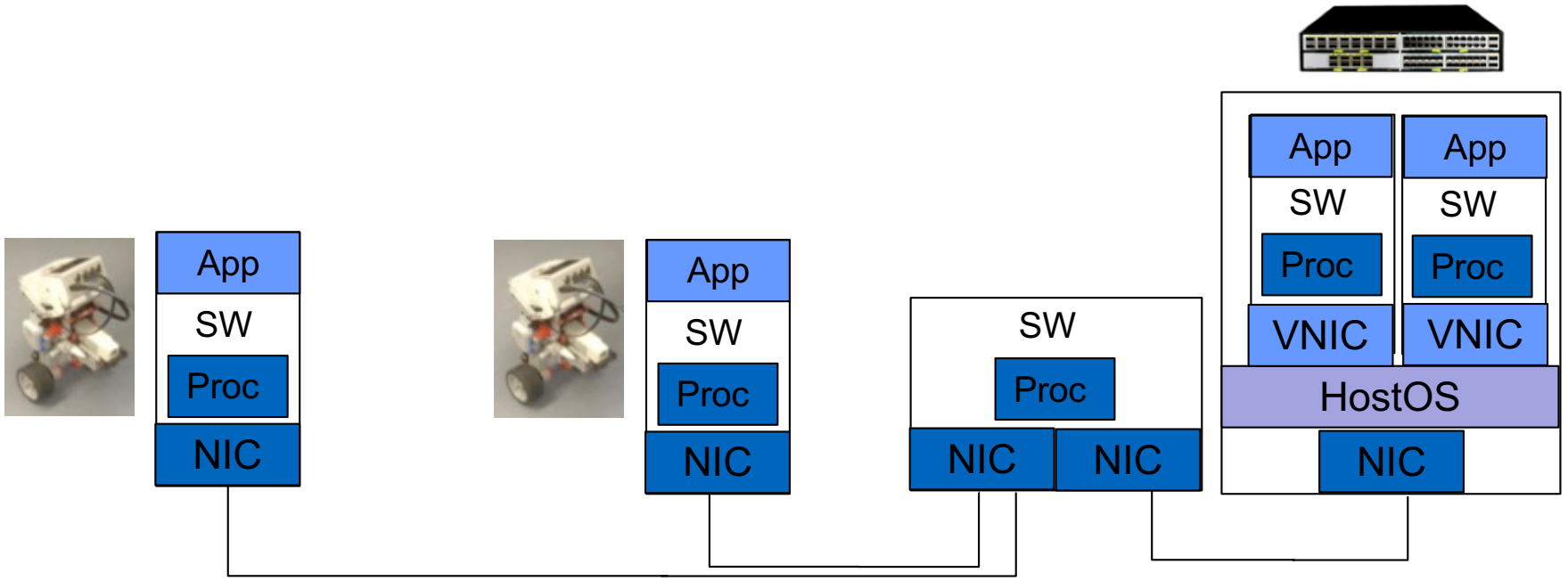
Goal:

- Predictable performance of networked systems

Challenges:

- Complex Hardware + Software
- Programmability
- Issue: latency distribution (long tail)





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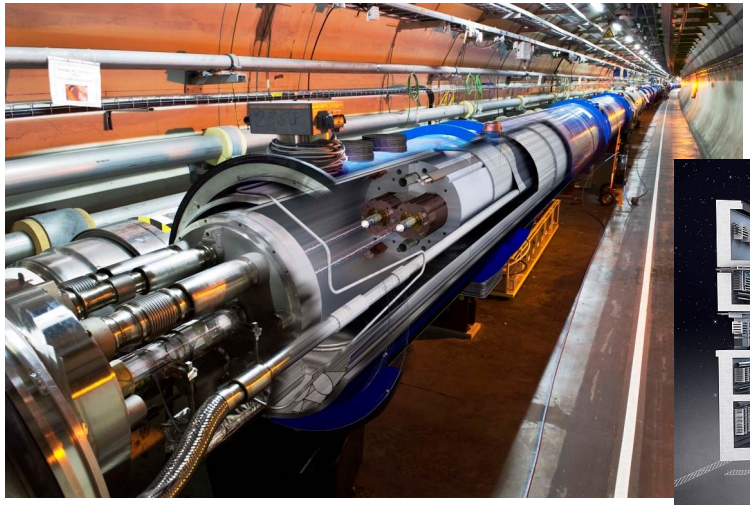
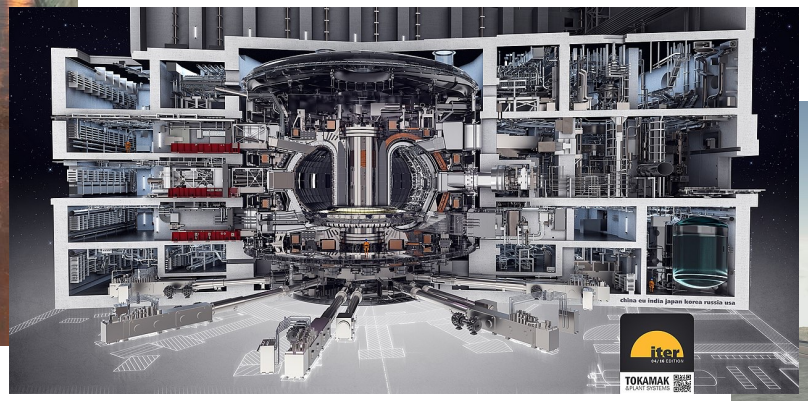
Goal:

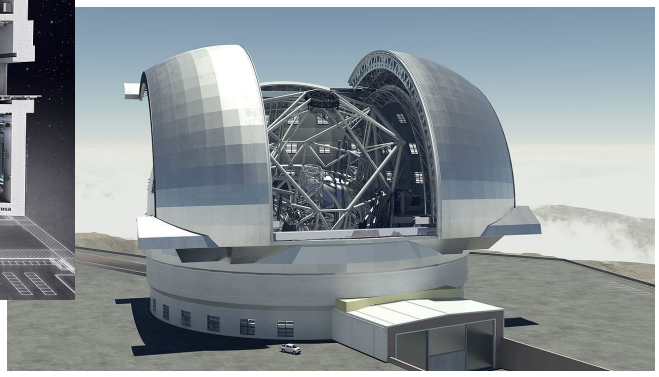
Research Infrastructure for Networked Systems

Natural Sciences Research infrastructures

- Large-scale research infrastructures have become a necessity to answer current research questions
- Long-term funding programs allow the creation of infrastructures
  - Large Hadron Collider
  - Fusion Reactor ITER
  - Extremely Large Telescope
- Which is the right research infrastructure for Computer Science?







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Challenge: Complexity

Complexity of Protocol Stack

Complexity by Programmability

Complexity by Processing Architecture

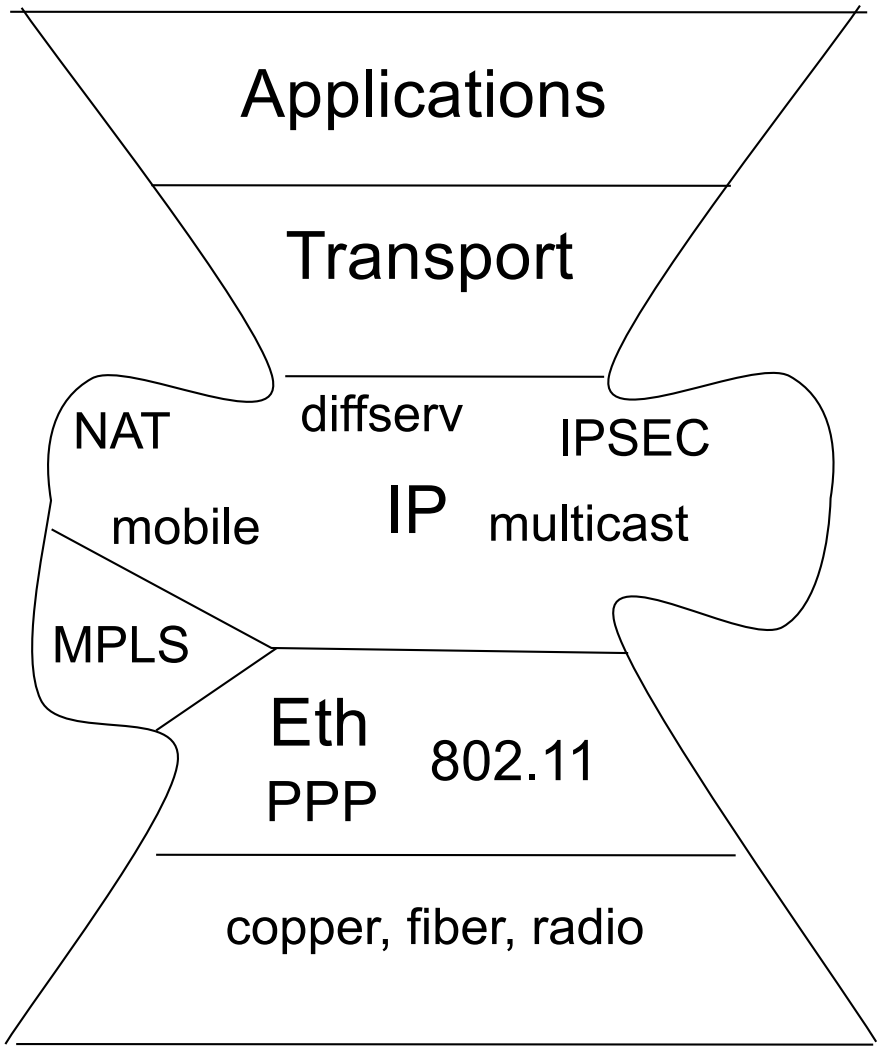
Complexity by Software Architecture

Latency Guarantees

Reproducible Experiments

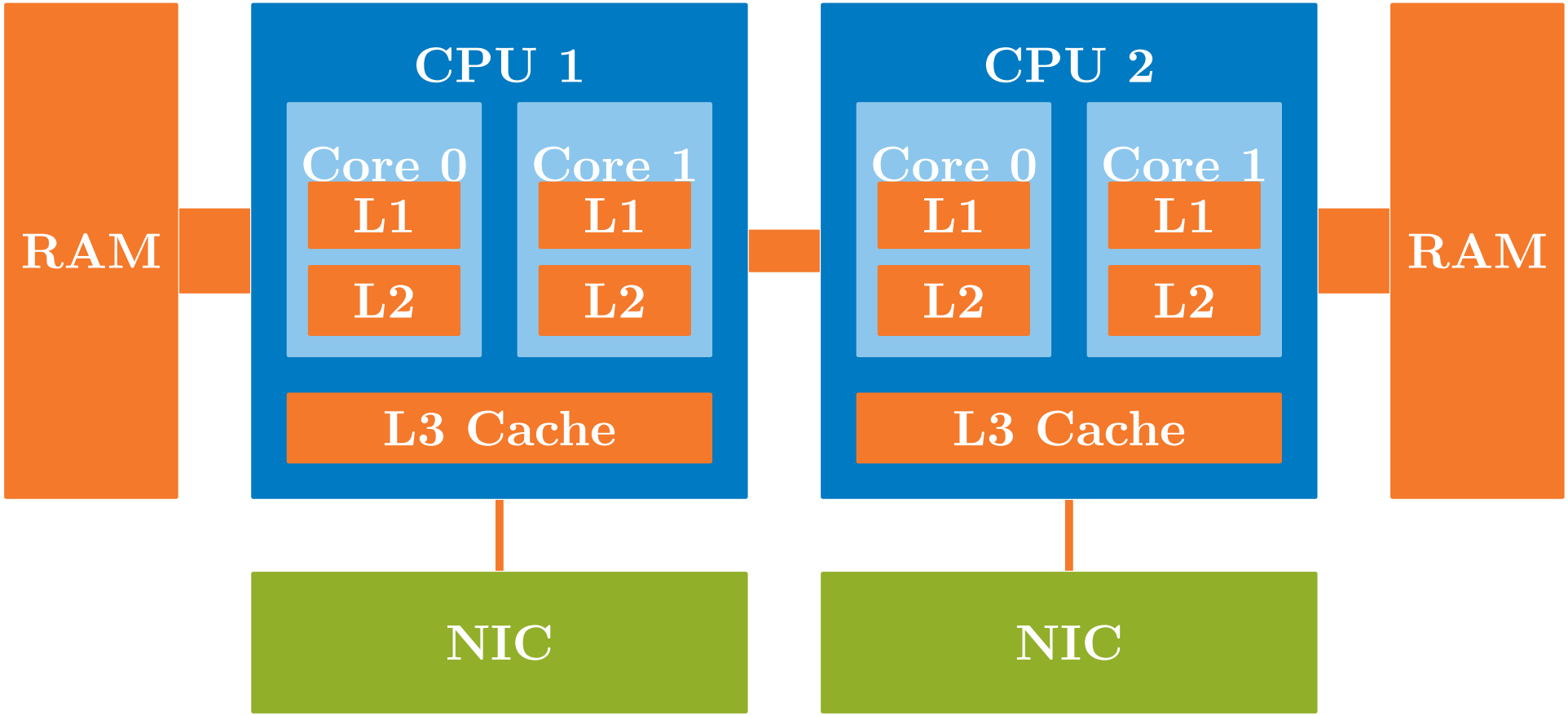
Protocol Stacks are Complex

- TLS, QUIC, MASQUE
- TCP, UDP
- BGP, OSPF,
  VRRP, PIM
- IPsec, IKE, EAP
- IPv4, IPv6, Segment Routing
- VLAN, GTP, IP in IP, GRE, MPLS

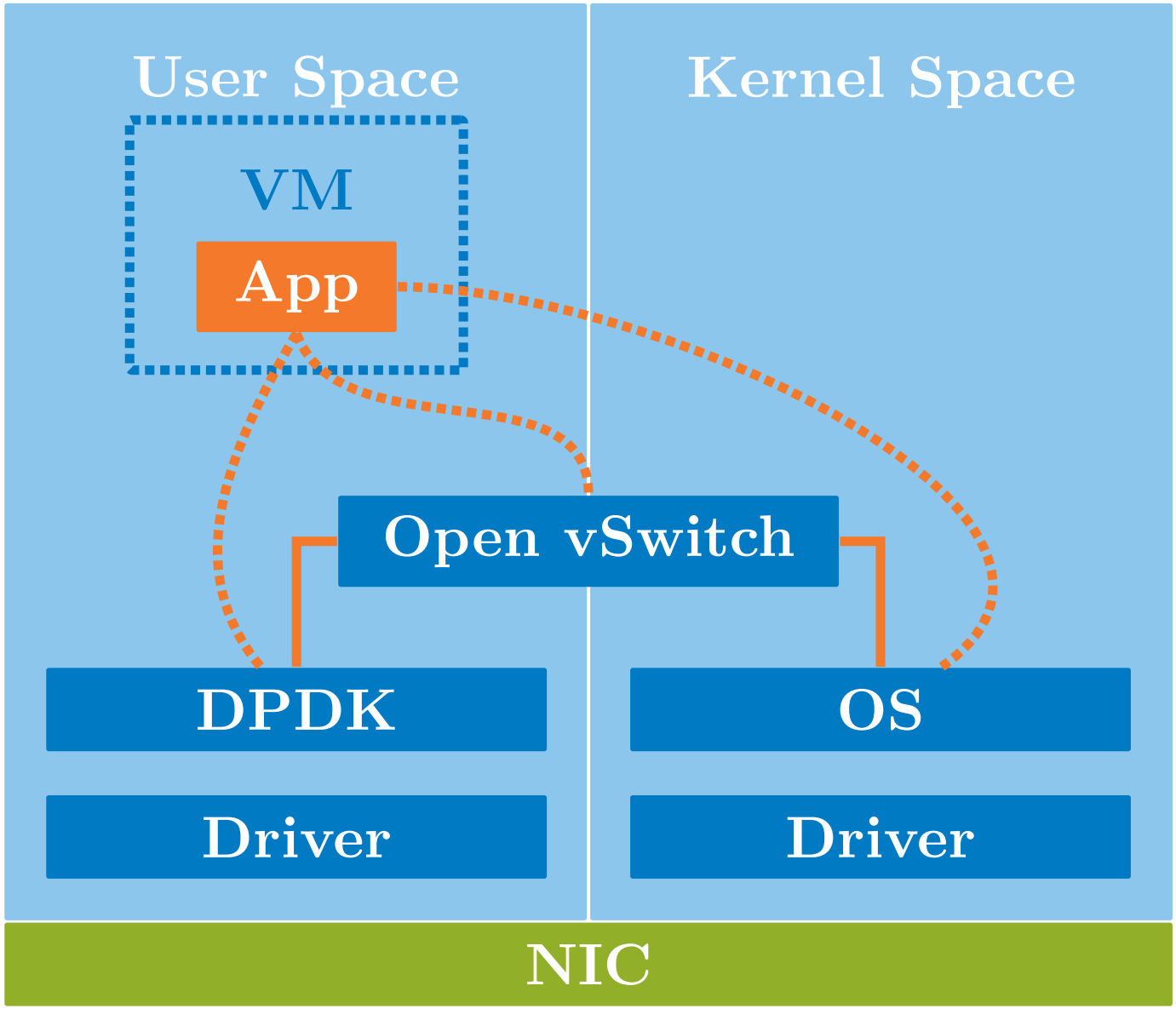


Modern Hardware Architectures are Complex

Non-Uniform Memory Architecture (NUMA)



Modern Software Architectures are Complex

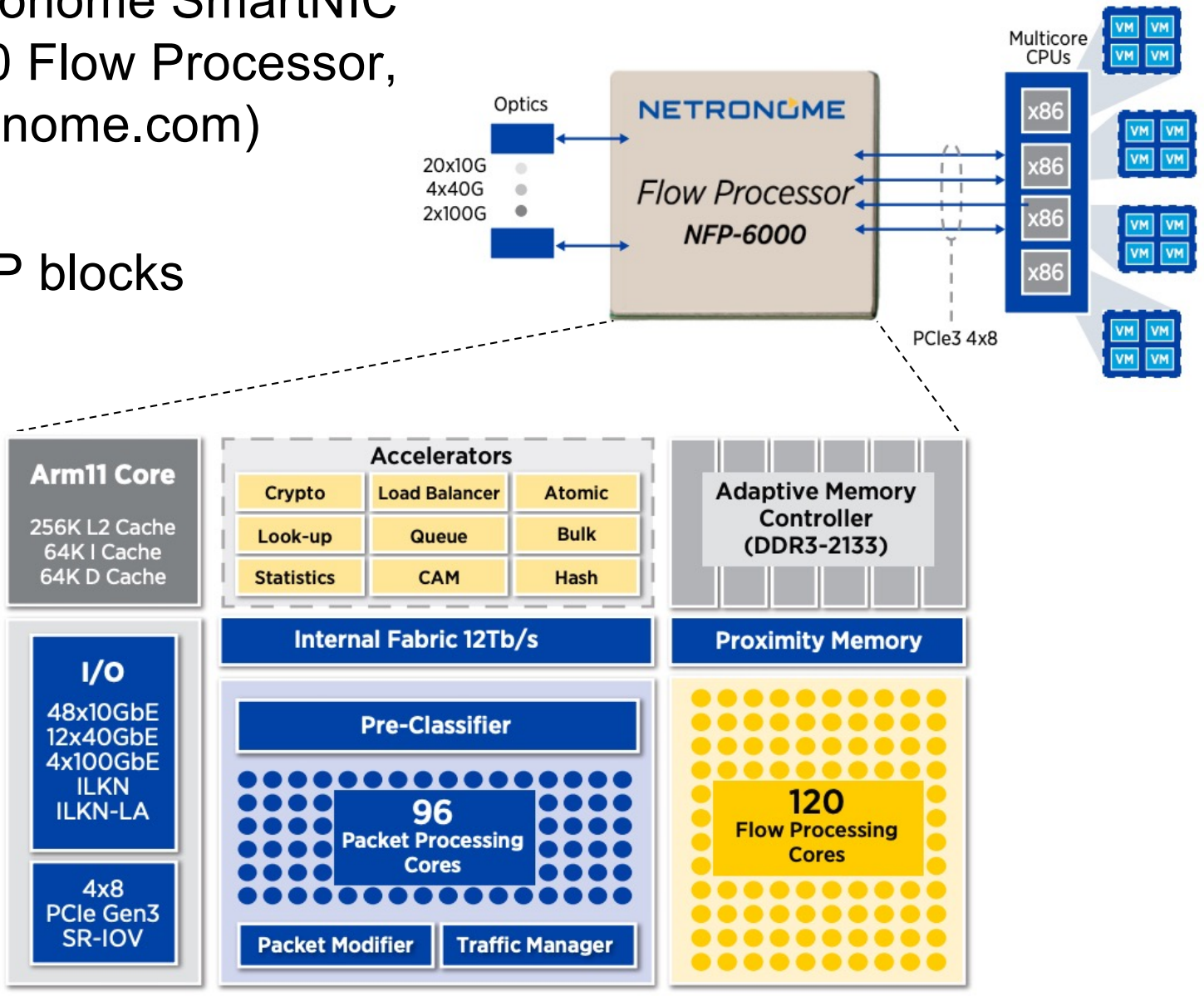


Programmable NICs add Complexity

Programmable packet processing architectures
Example: Netronome SmartNIC
with NFP-6000 Flow Processor,
(cf. www.netronome.com)

NICs

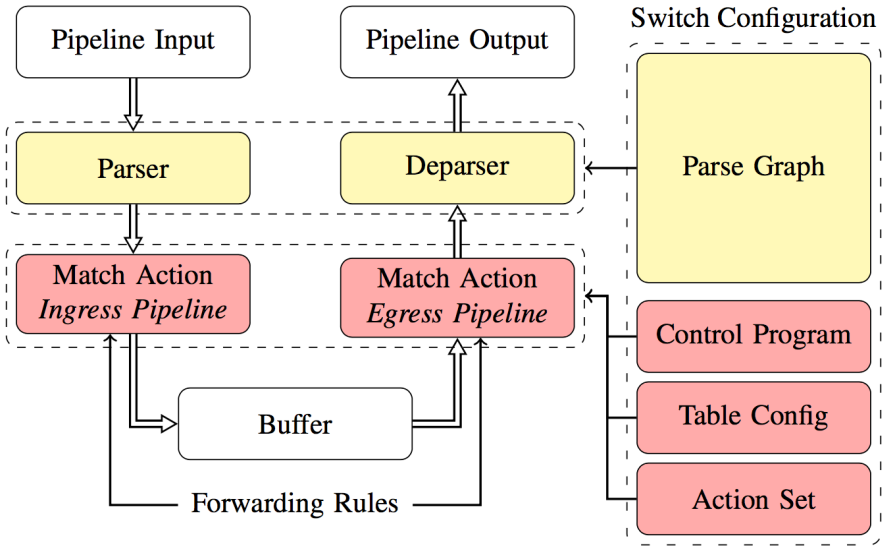
Composable IP blocks



P4 Programmable Packet Processing adds Complexity

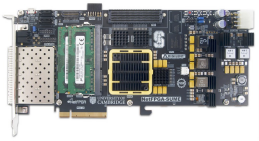
P4 Architecture

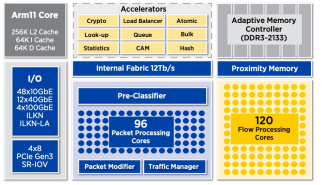
Programmable High-Performance Packet Processing

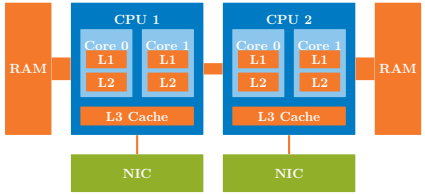


P4 on different processing targets

- Tofino ASIC-based switch
- P4NetFPGA
- P4 Programming of SmartNIC
- P4 Programming of CPUs (t4p4s DPDK)





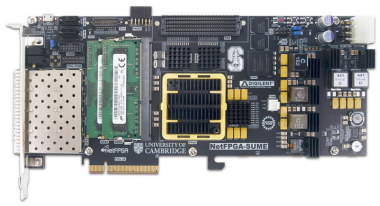


P4 Programmable Network Devices

Comparison of P4 Programmable Target Types

	CPU	NPU	FPGA	ASIC
Throughput	+	++	+++	++++
Latency	> 10 µs	5 µs to 10 µs	< 2 µs	< 2 µs
Jitter	----	---	--	-
Resources	++++	+++	++	+
Flexibility	++++	+++	++	+
Example	t4p4s DPDK	NFP-4000 SmartNIC	NetFPGA SUME	Intel Tofino



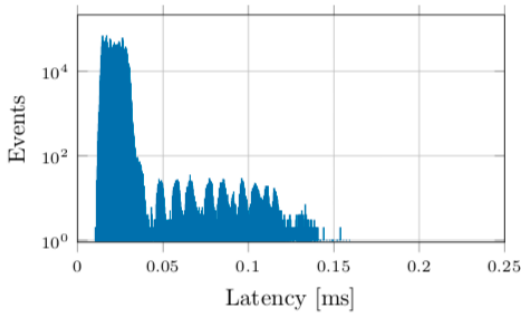



[ITC2020] Dominik Scholz, Henning Stubbe, Sebastian Gallenmüller, Georg Carle, "Key Properties of Programmable Data Plane Targets," in 32nd International Teletraffic Congress (ITC 32), Osaka, Japan, Sep. 2020

Digital Sovereignty Contribution: High-performance low-latency systems Programmable with P4, realized using multiple target types, from different vendors

Challenge: Providing Latency Guarantees

Networked system with programmable network components:



App
SW
Proc
NIC

App
SW
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NIC

SW
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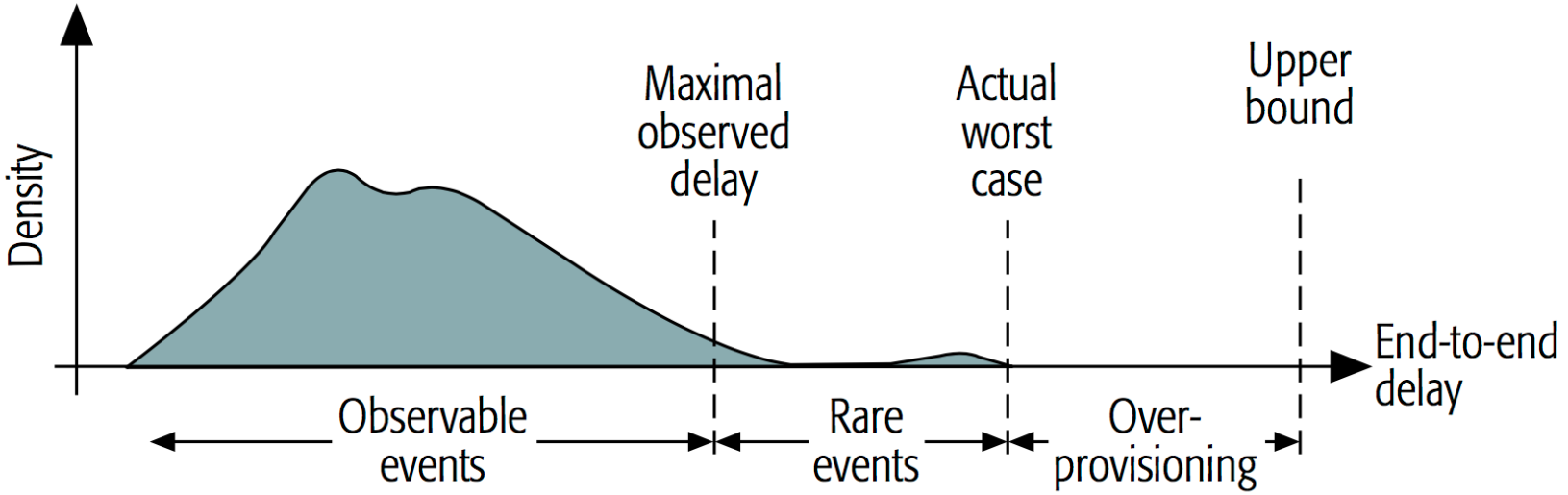
NIC
NIC

App
App
SW
SW
Proc
Proc
VNIC
VNIC
HostOS
NIC

Maximal observed delay vs. upper bound:



[CommsMag] Fabien Geyer, Georg Carle: Network engineering for real-time networks: Comparison of automotive and aeronautic industries approaches, IEEE Communications Magazine 54 (2), 2016

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Reproducible Experiments

Viewpoints on Reproducible Research

ACM SIGCOMM MoMeTools - Workshop on Models, Methods and Tools for Reproducible Network Research
Georg Carle, Hartmut Ritter, Klaus Wehrle,
Karlsruhe, Germany, August 2003

ACM SIGCOMM Reproducibility Workshop
Olivier Bonaventure, Luigi Iannone, Damien Saucez
Los Angeles, USA, August 2017

[Rep17] Q. Scheitle, M. Wählisch, O. Gasser, T. Schmidt, G. Carle,
Towards an ecosystem for reproducible research in computer networking
Proceedings of the ACM SIGCOMM Reproducibility Workshop, 2017

Dagstuhl seminar 18412 "Encouraging Reproducibility in Scientific Research of the Internet", October 2018

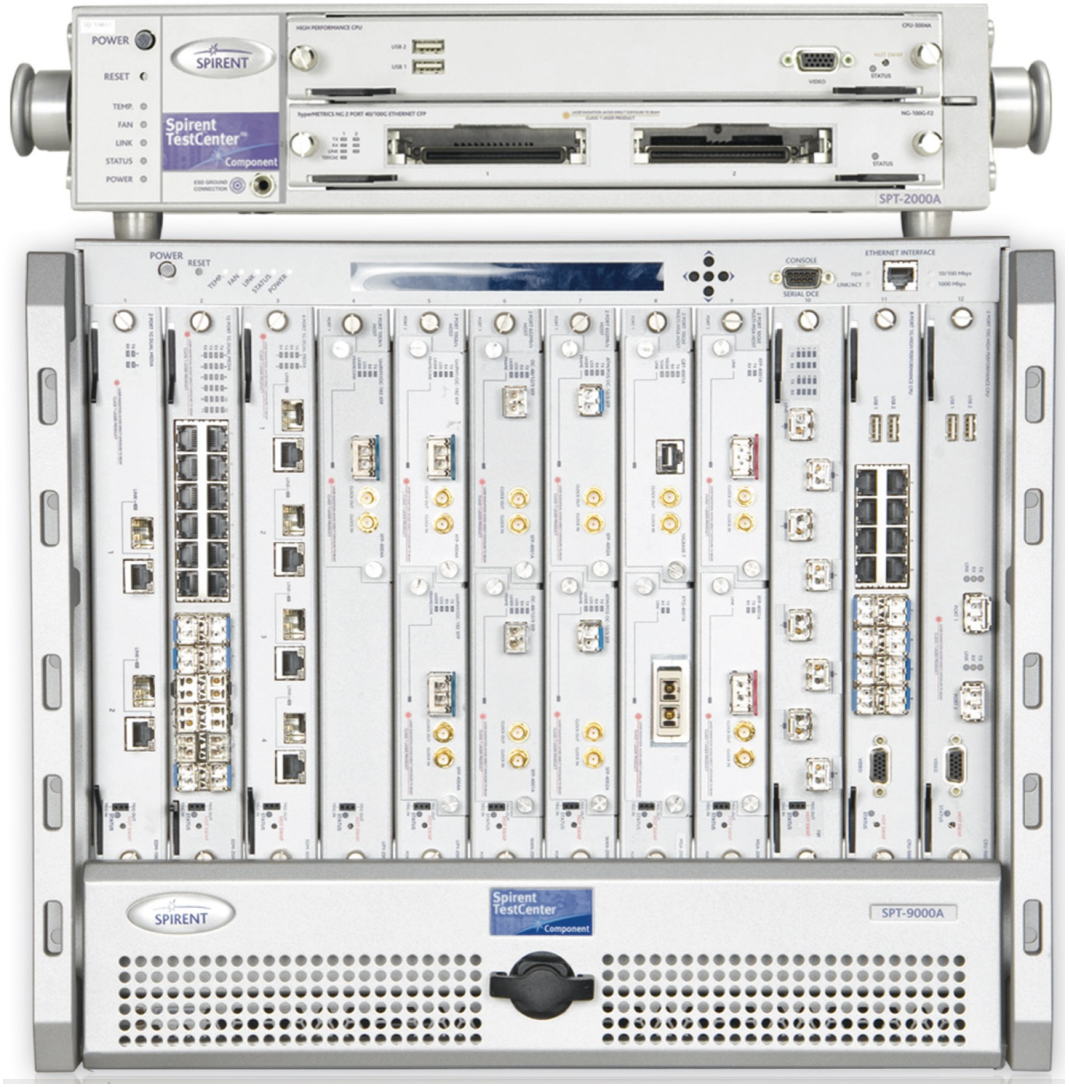
- Despite 20 years since first workshop have passed, hard problems remain
- Current approaches
  - Artifact evaluation committees
  - Reproducibility badges
- Remaining problems
  - High effort for researchers to make research reproducible
  - High effort for members of artifact evaluation committee to validate reproducibility
  - Low robustness of experimental results due to insufficient documentation

Hardware Traffic Generators

- Fast
- Precise

but

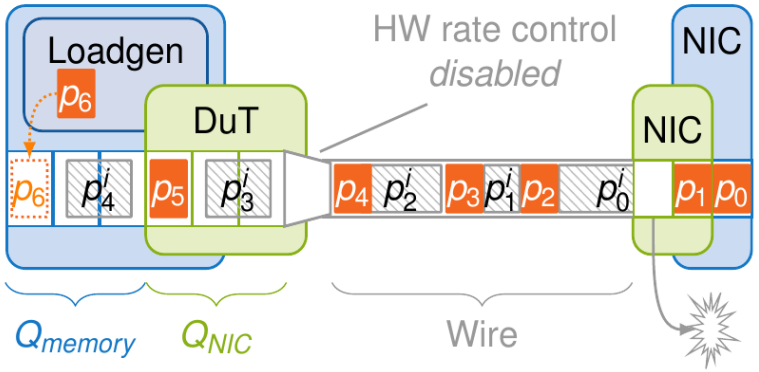
- Expensive
- Difficult to deploy
- Inflexible



Spirent traffic generator

MoonGen

- Inexpensive: Commercial Off-The-Shelf hardware
- Fast: DPDK for packet I/O, multi-core support
- Easy to deploy: simple software setup
- Flexible: user-controlled Lua scripts
- Precise
  - Timestamping: Utilize hardware features of commodity NICs
  - Rate control: Hardware features and software approach
  - Inter-packet spacing: gaps filled with invalid frames



[IMC15] Paul Emmerich, Sebastian Gallenmüller, Daniel Raumer, Florian Wohlfart, Georg Carle: MoonGen: A Scriptable High-Speed Packet Generator, ACM SIGCOMM Internet Measurement Conference (IMC), Oct. 2015

[ANRP17] Internet Research Task Force (IRTF) Applied Networking Research Prize, IETF-100, Nov. 2017, https://irtf.org/anrp

[ANCS17] Paul Emmerich, Sebastian Gallenmüller, Gianni Antichi, Andrew Moore, Georg Carle: Mind the Gap – A Comparison of Software Packet Generators, ACM/IEEE Symposium on Architectures for Networking and Communications Systems 2017

Questions?